IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Simplified model and submodule capacitor voltage balancing of single-phase AC/AC modular multilevel converter for railway traction purpose

ISSN 1755-4535
Received on 20th February 2015
Revised on 16th October 2015
Accepted on 22nd October 2015
doi: 10.1049/iet-pel.2015.0120
www.ietdl.org

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Abstract: A single-phase AC/AC modular multilevel converter (MMC) can interact directly with 25 kV railway grid without a bulky 50 Hz step-down transformer. This brings in great savings in size and cost. Submodule (SM) voltage balancing of this kind of MMCs remains a major technique issue. This study proposes a voltage-balancing solution for this scenario which consists of intra- and inter-arm voltage balancing methods. The former combines the advantages of carrier phase-shifted pulse-width modulation (PWM) and phase disposition PWM based voltage-balancing methods. It only uses two proportional regulators, easing the control system significantly. The latter is based on a power channel between the upper and lower arms. It avoids interferences with input/output voltage and current, and gets rid of common mode current component which would be injected into the grid with conventional inter-arm balancing methods. By assuming perfect voltage-balancing, a simplified mathematical model is also developed, which reveals more clearly the power conversion relationship. Simulations and experiments verify the proposed voltage-balancing methods and the mathematical model.

Nomenclature

C	capacitance of each SM capacitor
N	number of SMs in one arm
U_C	SM capacitor voltage
T_c	carrier period
T_o	output fundamental period
U_{T1}, U_{T2}	voltages across primary and secondary windings of transformer, respectively
U_{UCi}, U_{LCi}	voltage of the 'ith' SM capacitor in upper arm and lower arms, respectively, $i = 1, 2, \ldots, N$
u_U, u_L, i_U, i_L	voltage and current of upper and lower arms, respectively
u_S, i_S, f_S	grid voltage, current, and frequency
u_o, i_o, f_o	output voltage, current, and frequency
U_{CU}^{Σ}, U_{CL}^{Σ}	sums of SM capacitor voltages of the upper and lower arms
$\bar{U}_U^{\Sigma}$, $\bar{U}_L^{\Sigma}$	averaged SM capacitor voltages of the upper and lower arms

1 Introduction

Among various multilevel converter topologies, the modular multilevel converter (MMC) [1] has become the most promising one due to advantages such as perfect modularity with identical individual cells, distributed energy storage, simple voltage scaling, possibility of a common DC bus configuration, simple realisation of redundancy, flexibility for choosing a grid side converter, and so on. In the recent decade, a lot of research on the MMC has been done, with the application areas ranging from high-voltage direct current (HVDC), STATCOM, renewable energy utilisation to medium voltage (MV) drives [2–6]. However, research work on application of single-phase AC/AC MMCs for railway traction drives is relatively limited [7]. This paper concentrates on railway traction application of the MMC, where the MMC is connected with the 25 kV/50 Hz railway grid without a transformer. The MMC outputs a medium-frequency square-wave voltage, which can be processed by a much smaller, medium-frequency isolation transformer. The secondary winding of the isolation transformer can be connected to a traditional traction converter. The schematic of such a traction drive is shown in Fig. 1*a*.

Each phase/leg of the MMC is composed of many identical submodules (SMs). It is important to keep the SM capacitor voltages in balance within each phase, since proper operation of the MMC is based on this assumption. However in practical operations, an MMC is prone to SM voltage imbalance. Taking the pulse-width modulation (PWM) strategies often used with MMCs for example, the phase disposition PWM (PDPWM) causes voltage imbalance naturally (due to its uneven distribution of switching frequencies). For the carrier phase-shifted PWM (CPSPWM), voltage imbalance can also occur due to differences in component parameters (device losses, capacitances, etc.) and control actions among different SMs. Without proper balancing control, the voltage imbalance among the SMs can go beyond certain limit and cause a lot of problems, such as uneven distribution of losses among the power devices switches, overvoltage of some SMs, distorted output voltage waveform, or even instability of the MMC system. Therefore, voltage balancing has become a major research interest for various kinds of MMCs.

Voltage-balancing task can be divided into two subtasks: (i) keep the SM voltages within each arm even; (ii) keep the total SM voltages of the upper and lower arms even. These are called intra-arm and inter-arm voltage balancing, respectively, in this paper. As to the intra-arm voltage balancing, there are mainly two groups of methods found in the literature: CPSPWM-based methods [8] and PDPWM-based methods [9–13]. There are also other intra-arm voltage-balancing methods [14–16], but with relatively less applications.

In CPSPWM-based methods [8], intra-arm voltage balancing is achieved with $2N$ (N being the number of SMs within one arm)

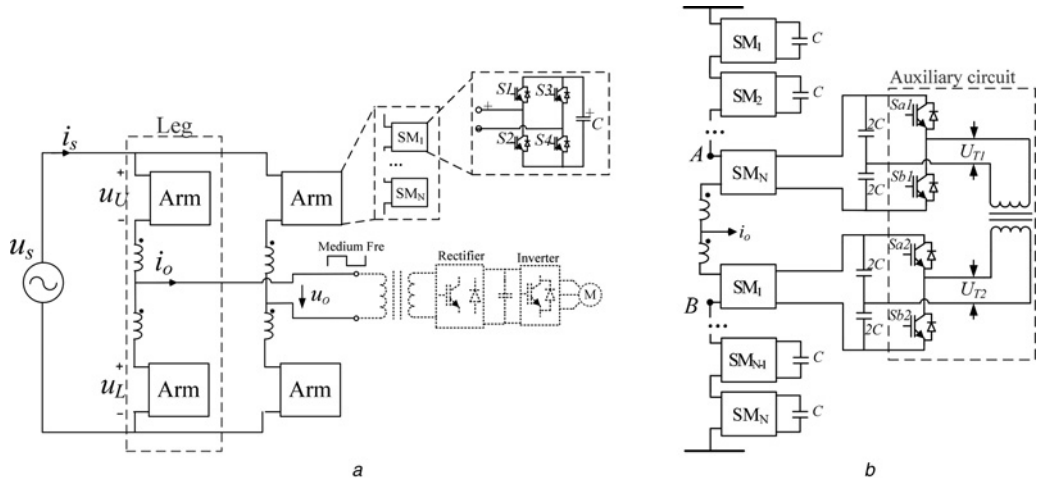

Fig. 1 *Schematic of a traction drive*

a Topology of the single-phase AC–AC MMC for railway traction drives
b Auxiliary circuit for proposed inter-arm balancing (same for the other leg)

proportional regulators fed by the errors between SM capacitor voltages and their references in one leg. These regulators then minimise the errors by changing the modulating signals of the SMs. However, with the increase of the number of SMs, the number of SM-level balancing regulators and PWM comparators also increases, which raises the hardware and software cost significantly. Besides, changing the modulating signals of the SMs may affect the input/output power quality.

PDPWM is used extensively in MMCs due to its easy implementation. However, an intrinsic feature of PDPWM is uneven distribution of switching frequencies among the SMs within one arm, which gives rise to an uneven distribution of switching losses among the SMs, and which causes severe voltage imbalance. To achieve the intra-arm balancing, methods based on voltage sorting algorithm are usually employed [9–13]. In those methods, capacitor voltages are measured and sorted during each carrier period. If the arm current is in charging direction, the SMs with highest voltages are given the priority to be turned off, and the SMs with lowest voltages are given the priority to be turned on. The opposite situation happens when the arm current is in discharging direction. In this way, SM voltages in one arm are balanced within a tight bound. However, since the aim of those methods is not equalising the switching frequencies among the SMs, the problem of uneven switching frequencies associated with PDPWM may still persist. Besides, altering the original distribution of gating signals in this way may introduce extra switching actions that are solely for the purpose of voltage balancing while totally unnecessary for output voltage synthesising [12]. These extra switching actions increase switching losses. On the other hand, the voltage sorting algorithm, which has to be executed every carrier period, poses a heavy computational burden, thus resulting in increased demand for hardware and software resource. In [12], an improvement is made such that only SMs currently 'off' are selected when extra SMs need to be turned on, and the opposite situation happens if extra SMs are to be turned off. This alleviates the extra switching problem to some extent. In [13], full sorting algorithm is avoided by taking care of the lowest and highest capacitor voltages only. Methods that can effectively deal with all three drawbacks mentioned above (i.e. uneven switching frequencies, extra switching actions, and computational burden) are yet to be found.

In this paper, a new intra-arm voltage-balancing method based on CPSPWM is proposed, which has the following features: (i) evenly distributed gating pulses for all SMs; (ii) no voltage sorting algorithm; (iii) only two balancing regulators for each arm; (iv) input/output power quality will not be affected; and (v) no need to monitor the direction of arm current.

For inter-arm voltage balancing (also called arm balancing), the existing solutions [8, 17, 18] can all be summarised as 'common mode injection' method. That is, a common mode (here the term 'common mode' means the signal is 'common' for upper and lower arms) component of the same frequency with the output is injected into both arms of one phase leg so as to exchange active power. However, for grid-connected systems, such as shown in Fig. 1*a*, the injected common mode current will flow into the grid and affect the input power quality.

In [19], power channels between upper and lower arms are introduced to overcome the low-frequency voltage fluctuation problem associated with MV drives. This concept can also be used for inter-arm voltage balancing. However, it is impractical to use N power channels here. This paper proposes a new inter-arm voltage-balancing method in which one power channel is introduced between the upper and lower arms. The power channel is basically a bidirectional DC/DC converter consisting of two half-bridge modules and a medium-frequency transformer. Active power is exchanged by means of phase-shifting control of the bidirectional DC/DC converter.

In addition to the voltage-balancing method, modelling and control of the MMC are also addressed in this paper. In [20], the author established a mathematical model based on state-space equations. In [21], an averaged model is established on the basis of individual SMs. As a result, the equivalent arm module is defined. However, these models are a bit complicated when describing in a macroscopic way the power relationship among the input, the output, and the SM capacitors. In [22], the model of the MMC is simplified with an equivalent boost–buck circuit. However, it does not apply easily to the system shown in Fig. 1*a*. In this paper, under the assumption that the intra-arm and inter-arm voltage balancing are both working well, an analogy of the main circuit shown in Fig. 1*a* to a traditional PWM rectifier followed by a PWM inverter is made. A much simplified and straightforward mathematical model of the main circuit is then established. Based on this model, existing control schemes for single-phase converters can be readily used to control the MMC shown in Fig. 1*a*.

The paper is organised as follows. A simplified mathematical model is established in Section 2. In Section 3, the proposed intra-arm and inter-arm voltage-balancing methods are presented. The complete control system for one phase leg of the MMC is given in Section 4. In Section 5, the proposed method is validated with simulation and experimental results.

2 Mathematical model

In this section, under the assumption of perfect capacitor voltage balancing, a simplified model of the MMC is established. The overall control system of the MMC consists of two layers: outer

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(input/output) control and inner (voltage balancing) control. The former can be easily designed based on the established model.

Equivalent circuit of one phase leg of the MMC is shown in Fig. 2*a*. According to Kirchhoff's voltage law

$$\frac{u_s}{2} = L\frac{\mathrm{d}i_\mathrm{U}}{\mathrm{d}t} + M\frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t} + i_\mathrm{U}R + u_\mathrm{U} + u_\mathrm{o} \tag{1}$$

$$\frac{u_s}{2} = L\frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t} + M\frac{\mathrm{d}i_\mathrm{U}}{\mathrm{d}t} + i_\mathrm{L}R + u_\mathrm{L} - u_\mathrm{o} \tag{2}$$

Adding and subtracting (2) from (1) yield

$$(L+M)\frac{\mathrm{d}(i_\mathrm{U}+i_\mathrm{L})}{\mathrm{d}t} + (i_\mathrm{U}+i_\mathrm{L})R = u_s - (u_\mathrm{U}+u_\mathrm{L}) \tag{3}$$

$$(L-M)\frac{\mathrm{d}(i_\mathrm{U}-i_\mathrm{L})}{\mathrm{d}t} + (i_\mathrm{U}-i_\mathrm{L})R = -(u_\mathrm{U}-u_\mathrm{L}) - 2u_\mathrm{o} \tag{4}$$

Suppose

$$\begin{cases} u_\mathrm{U} + u_\mathrm{L} = 2u_\mathrm{com} \\ u_\mathrm{U} - u_\mathrm{L} = -2u_\mathrm{diff} \end{cases} \tag{5}$$

where u_com and u_diff are the common-mode and differential-mode components of the upper- and lower-arm voltages.

Solving (5) for u_U and u_L gives

$$\begin{cases} u_\mathrm{U} = u_\mathrm{com} - u_\mathrm{diff} \\ u_\mathrm{L} = u_\mathrm{com} + u_\mathrm{diff} \end{cases} \tag{6}$$

The current relationship is as follows:

$$i_\mathrm{U} - i_\mathrm{L} = i_\mathrm{o} \tag{7a}$$

$$i_\mathrm{U} + i_\mathrm{L} = 2i_s \tag{7b}$$

where i_s is usually called circulating current. Substituting (7) into (3) and (4) yields

$$2(L+M)\frac{\mathrm{d}i_s}{\mathrm{d}t} + 2Ri_s = u_s - (u_\mathrm{U}+u_\mathrm{L}) = u_s - 2u_\mathrm{com} \tag{8a}$$

$$(L-M)\frac{\mathrm{d}i_o}{\mathrm{d}t} + Ri_\mathrm{o} = -(u_\mathrm{U}-u_\mathrm{L}) - 2u_\mathrm{o} = 2u_\mathrm{diff} - 2u_\mathrm{o} \tag{8b}$$

u_U and u_L can be seen as obtained by modulating U_CU^Σ (total SM capacitor voltage of the upper arm) and U_CL^Σ (total SM capacitor voltage of the lower arm), respectively

$$u_\mathrm{U} = u_{r\mathrm{U}}U_\mathrm{CU}^\Sigma = (u_{rs} - u_{ro})U_\mathrm{CU}^\Sigma \tag{9a}$$

$$u_\mathrm{L} = u_{r\mathrm{L}}U_\mathrm{CL}^\Sigma = (u_{rs} + u_{ro})U_\mathrm{CL}^\Sigma \tag{9b}$$

where $u_{r\mathrm{U}}$, $u_{r\mathrm{L}}u_{rs}$, u_{ro} are the modulating signals corresponding to u_U, u_L, u_com, u_diff, respectively. Due to the inner control that will be discussed in next section

$$U_\mathrm{CU}^\Sigma = U_\mathrm{CU}^\Sigma = \frac{U_\mathrm{C}^\Sigma}{2} \tag{10}$$

where U_C^Σ is the total capacitor voltage of one phase leg. By taking (9) and (10) into consideration, (8) is changed into (11)

$$2(L+M)\cdot\frac{\mathrm{d}i_s}{\mathrm{d}t} + 2R\cdot i_s = u_s - u_{rs}U_\mathrm{C}^\Sigma \tag{11a}$$

$$\frac{L-M}{2}\cdot\frac{\mathrm{d}i_\mathrm{o}}{\mathrm{d}t} + \frac{R}{2}\cdot i_\mathrm{o} = \frac{u_\mathrm{ro}U_\mathrm{C}^\Sigma}{2} - u_\mathrm{o} \tag{11b}$$

Equation (11a) is similar to the relationship of a single-phase PWM rectifier, that is, if we look u_s as the source voltage and $u_{rs}U_\mathrm{C}^\Sigma$ as the AC-side voltage of rectifier. A similar analogy can be made between (11b) and relationship of a single-phase PWM inverter, with $u_\mathrm{ro}U_\mathrm{C}^\Sigma/2$ being the AC-side voltage of the inverter and u_o the load voltage. These two converters exchange power via total leg capacitor $C_\mathrm{leg} = C/2N$.

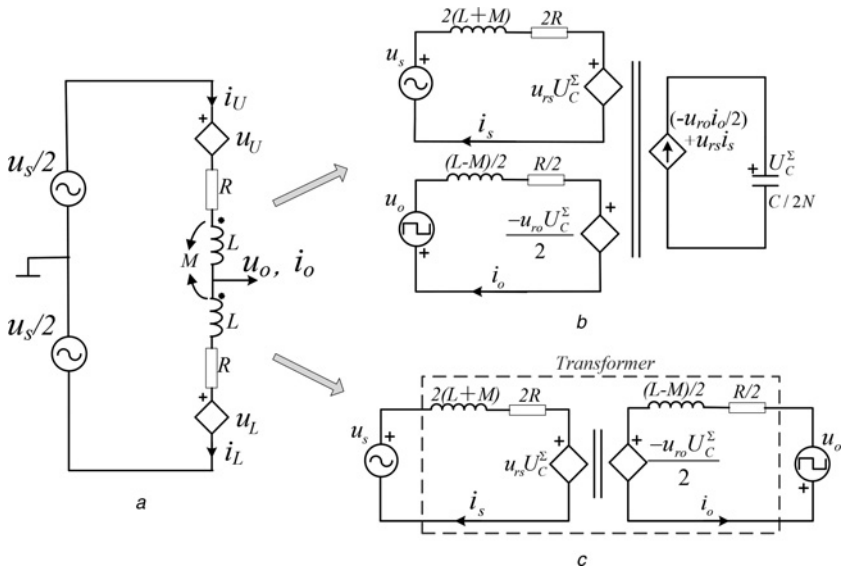

Fig. 2 *Equivalent circuit of one phase leg of the MMC*

a Equivalent circuit
b Simplified circuit model
c Further simplified 'VVVF transformer' model of one leg of the MMC

According to the working principle of the MMC, dynamic equations for arm capacitor voltages U_{CU}^{Σ} and U_{CL}^{Σ} are

$$\frac{C}{N}\frac{\mathrm{d}U_{\mathrm{CU}}^{\Sigma}}{\mathrm{d}t} = u_{r\mathrm{U}} i_{\mathrm{U}} \tag{12a}$$

$$\frac{C}{N}\frac{\mathrm{d}U_{\mathrm{CL}}^{\Sigma}}{\mathrm{d}t} = u_{r\mathrm{L}} i_{\mathrm{L}} \tag{12b}$$

With (10) and (12), dynamic equation for leg capacitor voltage U_{C}^{Σ} can be derived as

$$\frac{C}{2N}\frac{\mathrm{d}U_{\mathrm{C}}^{\Sigma}}{\mathrm{d}t} = u_{rs} i_s + \left(-u_{r\mathrm{o}}\frac{i_{\mathrm{o}}}{2}\right) \tag{13}$$

On the basis of (10) and (11), an equivalent circuit of Fig. 2*a* can be derived as shown in Fig. 2*b*. In Fig. 2*b*, the u_s loop is analogous to a PWM rectifier, the u_{o} loop is analogous to a PWM inverter, and the leg capacitor loop is analogous to the common DC link that links the two converters. Fig. 2*b* clearly demonstrates the power flow relationship among the input, the output, and the SM capacitors. Just like a conventional back-to-back PWM converter system, the power flow can also be reversed. From the input/output point of view, Fig. 2*b* can be further simplified into Fig. 2*c*, which can be seen as a variable-voltage variable-frequency (VVVF) transformer, with the rectifier part on the primary side and the inverter part on the secondary side.

3 Capacitor voltage-balancing control (inner control)

The simple and straightforward MMC model presented in the previous section depends on proper functioning of the balancing control of the SM capacitors' voltages, the aim of which is to make the total leg capacitor voltage U_{C}^{Σ} evenly distributed among all SM capacitors of that phase leg. This is also called 'inner control' in this paper, as compared with the 'outer control' which deals with the control of input current, output voltage as well as total leg capacitor voltage of the MMC, and which will be discussed in next section. As described in Section 1, SM capacitor voltage-balancing control (i.e. inner control) can be further divided into intra-arm voltage balancing and inter-arm voltage balancing.

3.1 Intra-arm voltage balancing

Take the lower arm for instance. The power of the SMs is expressed as

$$p_{\mathrm{SM}} = U_{\mathrm{C}}(u_{rs} + u_{r\mathrm{o}} + u_x)\cdot\left(i_s - \frac{i_{\mathrm{o}}}{2}\right) \tag{14}$$

where u_x is an added modulating component for voltage balancing. Equation (14) can be rewritten as

$$p_{\mathrm{SM}} = U_{\mathrm{C}}(u_{rs} + u_{r\mathrm{o}})\cdot\left(i_s - \frac{i_{\mathrm{o}}}{2}\right) + U_{\mathrm{C}}u_x\cdot\left(i_s - \frac{i_{\mathrm{o}}}{2}\right) \tag{15}$$

The second term on the right side of (15) contains average power if u_x is of the same frequency as i_s or i_{o}. This is the idea of most intra-arm voltage-balancing methods.

The proposed intra-arm voltage-balancing method will be used with CPSPWM, in which the gating pulses are evenly distributed among all SMs, and which results in relatively small imbalance compared with PDPWM. Thus, it is unnecessary to regulate all SMs of one arm. Here, only the two SMs with the highest and lowest voltages are compensated. The compensating signal, which contains the direction of the output current, is added to the modulating signal of the SM with the highest voltage, and subtracted from the SM with the lowest voltage, making the former discharged and the latter charged. The modulating signals of the two SMs after compensation are expressed as

$$u'_{r\_\mathrm{high}} = u_{rs} + u_{r\mathrm{o}} + \Delta d \tag{16a}$$

$$u'_{r\_\mathrm{low}} = u_{rs} + u_{r\mathrm{o}} - \Delta d \tag{16b}$$

where $\Delta d = \Delta D\cdot i_{\mathrm{o}}/|i_{\mathrm{o}}|$ is the compensating signal, the amplitude of which is

$$\Delta D = \frac{(U_{\mathrm{C\_high}} - U_{\mathrm{C\_low}})C}{2I_{\mathrm{o}}T_{\mathrm{o}}} \tag{17}$$

In which T_{o} is the output current period, $U_{\mathrm{C\_high}}$ and $U_{\mathrm{C\_low}}$ are the highest and lowest SM voltages, I_{o} is the amplitude of output current i_{o}. Derivation of (17) is based on the idea that the voltage difference is to be compensated in one output fundamental period, although the algorithm is implemented at carrier frequency.

On the basis of (15) and (16), powers of the two SMs are derived in (18). Note that power terms that do not contain average components are neglected for simplicity

$$p_{\mathrm{SM\_high}} = u_{rs}U_{\mathrm{C}}i_s - u_{r\mathrm{o}}U_{\mathrm{C}}\frac{i_{\mathrm{o}}}{2} + \Delta d\cdot U_{\mathrm{C}}\cdot\frac{i_{\mathrm{o}}}{2} \tag{18a}$$

$$p_{\mathrm{SM\_low}} = u_{rs}U_{\mathrm{C}}i_s - u_{r\mathrm{o}}U_{\mathrm{C}}\frac{i_{\mathrm{o}}}{2} - \Delta d\cdot U_{\mathrm{C}}\cdot\frac{i_{\mathrm{o}}}{2} \tag{18a}$$

The DC components of the first two terms on the right sides of (18a) and (18b) correspond to input and output power of the MMC, which normally cancel each other. The DC components of the third terms on the right sides serve the purpose of voltage balancing. As a result, voltage of the SM with highest voltage will decrease whereas the SM with lowest voltage will increase. By doing so, all capacitors' voltages within one arm can be regulated within a tight bound. It is important to note that the arm voltage would not be affected because the compensating signals for the two SMs are always complementary. Also note that the speed of voltage balancing would not be affected by the output current since the latter has been taken into account, as shown in (18). The schematic diagram of the proposed intra-arm balancing method is shown in Fig. 3*a*.

3.2 Inter-arm voltage balancing

It is necessary to briefly introduce the conventional inter-arm balancing method. Subtract (12b) from (12a), and consider

$$\begin{cases} u_{r\mathrm{U}} = \dfrac{(u_s/2 - u_{\mathrm{com}} - u_{\mathrm{diff}})}{U_{\mathrm{CU}}^{\Sigma}} \\ u_{r\mathrm{L}} = \dfrac{(u_s/2 - u_{\mathrm{com}} + u_{\mathrm{diff}})}{U_{\mathrm{CL}}^{\Sigma}} \end{cases} \tag{19}$$

Dynamic equation of the difference voltage between the upper and lower arms can be derived

$$\frac{C}{N}\frac{\mathrm{d}U_{\Delta}^{\Sigma}}{\mathrm{d}t} = \frac{C}{N}\frac{\mathrm{d}(U_{\mathrm{CU}}^{\Sigma} - U_{\mathrm{CL}}^{\Sigma})}{\mathrm{d}t} = \frac{u_s - 2u_{\mathrm{com}}}{2U_{\mathrm{C}}^{\Sigma}}i_{\mathrm{o}} - \frac{2u_{\mathrm{diff}}}{U_{\mathrm{C}}^{\Sigma}}i_s \tag{20}$$

In (20), if u_{com} contains output voltage component, or i_s contains output current component, both will produce average power to change the voltage-difference between upper and lower arm, which can be used for inter-arm balancing as the conventional method did. The problem is the approach will introduce output frequency component into the grid (see (3)).

In this paper, inter-arm balancing is carried out with an auxiliary circuit connecting one upper arm and one lower arm within each

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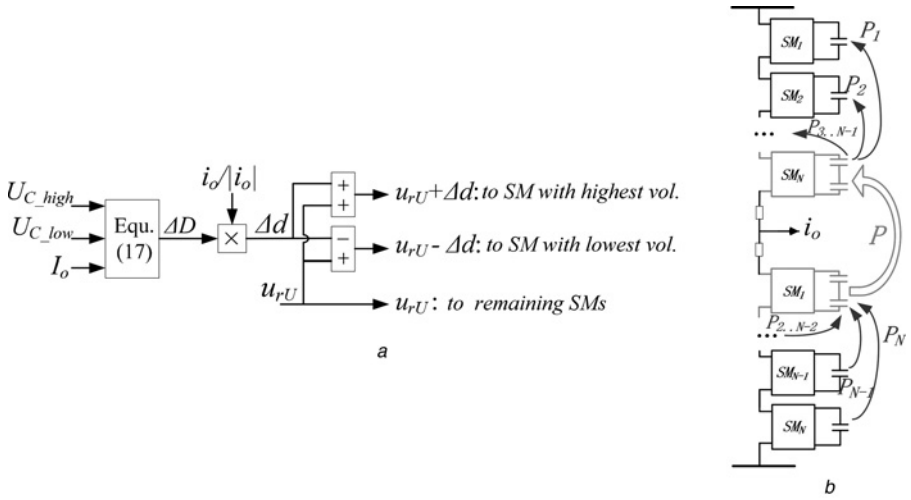

Fig. 3 *Schematic diagram of the proposed intra-arm balancing method*

a Schematic diagram for the proposed intra-arm voltage-balancing method (taking upper arm for example)

b Power flow with both intra-arm and inter-arm balancing methods when $\bar{U}_{\mathrm{U}}^{\Sigma} < \bar{U}_{\mathrm{L}}^{\Sigma}$

phase leg. The circuit, which is actually an isolated, bidirectional DC–DC converter, has already been shown in Fig. 1*b*. The proposed method has following features.

(i) Inter-arm balancing is now completely decoupled with arm voltage and current. Therefore, the input power quality will not be affected.
(ii) Only one such circuit is needed for a phase leg with $2N$ SMs.
(iii) Capable of zero voltage switching, the circuit features low switching loss.
(iv) The current stresses of the power devices in the auxiliary circuit are quite low, because the circuit only needs to transfer enough energy to eliminate the imbalance of the arm-capacitor voltages.
(v) By properly selecting the two SMs to be connected by the auxiliary circuit, insulation stress of the high-frequency transformer can be greatly reduced.

The power exchanged with the bidirectional DC–DC converter can be easily controlled by varying the phase-shift angle between the primary and secondary voltages, which are high-frequency square waves to reduce the size of the isolating transformer. The relationship between transmitted power and the phase-shift angle is as follows [23, 24]

$$P = \frac{U_{\mathrm{T1}} U_{\mathrm{T2}}}{\omega L} \varphi \left(1 - \frac{\varphi}{\pi}\right) \tag{21}$$

In (21), U_{T1}, U_{T2} are square-wave voltages amplitude of the transformer, ω is the frequency of the voltages, and φ is the phase-shift angle. The phase-shift angle is calculated according to the difference between the total capacitor voltages of the upper and lower arms, which is restricted in a range of $-\pi/2$ to $\pi/2$ to avoid multiple solutions.

The relationship between inter-arm power (P) and average SM capacitor voltages of the two arms ($\bar{U}_{\mathrm{U}}^{\Sigma}$, $\bar{U}_{\mathrm{L}}^{\Sigma}$) are based on the assumption that the energy transferred from one arm to the other are shared evenly among N SM capacitors of each arm by means of the intra-arm balancing control. Coordination of these two balancing actions will be discussed in more detail in the next subsection.

3.3 Coordination between inter-arm balancing and intra-arm balancing

Since only one DC–DC converter is used for each phase leg, the sent/received energy of the two connected SMs should be distributed to other $N-1$ SMs within the same arm in a timely fashion (by means of the intra-arm balancing method mentioned earlier in Section 3.1), otherwise severe intra-arm imbalance will arise. This basically requires that the power transmitted via the DC–DC converter (for inter-arm balancing purpose) should not exceed the maximum power (denoted as P_{m}) that can be exchanged between SMs with the highest and lowest capacitor voltages within each arm.

P_{m} is closely related to the modulation index m. Under rated condition, m is usually set around 0.9. A larger m leaves smaller room for modification of the modulating signal, thus smaller P_{m}. For the proposed intra-arm voltage-balancing method, P_{m} can be calculated as

$$P_{\mathrm{m}} = C\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t}u_{\mathrm{C}} \simeq C\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t}U_{\mathrm{C}} \simeq \frac{(1-m)U_{\mathrm{C}} \cdot I_{\mathrm{o}}}{2} \tag{22}$$

The corresponding maximum phase-shift angle for the auxiliary DC–DC converter is therefore

$$\varphi_{\mathrm{m}} = \frac{\pi - \sqrt{\pi^2 - 4a\pi}}{2}, \quad a = \frac{P_{\mathrm{m}}\omega L}{U_{\mathrm{C}}^2} \tag{23}$$

Fig. 3*b* depicts the capacitor voltage-balancing process of a whole phase leg taking into account the two balancing methods, where $\bar{U}_{\mathrm{U}}^{\Sigma} < \bar{U}_{\mathrm{L}}^{\Sigma}$ is assumed. As shown in Fig. 3*b*, excessive capacitor energy of the lower arm is transmitted from SM_1 of that arm to SM_N of the upper arm via the auxiliary DC–DC converter. Meanwhile, the sent energy of SM_1 of the lower arm is supplied from SM_2–SM_N of the same arm, and the received energy of SM_N in the upper arm is distributed to SM_1–SM_{N-1} of the same arm, with the proposed intra-arm balancing method.

3.4 Insulation issue of the transformer in the auxiliary circuit

It is necessary to reduce the voltage between the two windings of the isolating transformer in the auxiliary DC–DC converter. Otherwise, high insulation stress may raise the cost and/or shorten the life of the transformer. If only inter-arm power transfer is concerned, the DC–DC converter can be connected to any one SM of each arm. However, the insulation voltage can be totally different. For example, the whole grid voltage (25 kV in practice) will be imposed between the primary and secondary windings of the transformer when the auxiliary circuit is connected to SM_1 of the upper arm and

Table 1 Four combinations of N_U and N_L

	#1	#2	#3	#4
N_U	$\text{ceiling}\left(\frac{u_s/2-u_o}{U_C}\right)$	$\text{ceiling}\left(\frac{u_s/2-u_o}{U_C}\right)-1$	$\text{ceiling}\left(\frac{u_s/2-u_o}{U_C}\right)-1$	$\text{ceiling}\left(\frac{u_s/2-u_o}{U_C}\right)$
N_L	$\text{ceiling}\left(\frac{u_s/2+u_o}{U_C}\right)$	$\text{ceiling}\left(\frac{u_s/2+u_o}{U_C}\right)-1$	$\text{ceiling}\left(\frac{u_s/2+u_o}{U_C}\right)$	$\text{ceiling}\left(\frac{u_s/2+u_o}{U_C}\right)-1$

SM_N of the lower arm. A quick investigation of the MMC topology reveals that to reduce the voltage withstood by the transformer as much as possible, the auxiliary DC–DC converter has to be connected to the bottom SM (SM_N) in the upper arm and the top SM (SM_1) in lower arm, as already shown in Fig. 1*b*. The following derivation will prove that the maximum voltage imposed between the windings of the transformer is no higher than $4U_C$ with such a connection.

For most of the PWM strategies (PDPWM, CPSPWM, etc.), the numbers of inserted SMs for the upper and lower arms at any time of operation are

$$N_U = \text{ceiling}\left(\frac{u_s/2-u_o}{U_C}\right), \quad \text{or ceiling}\left(\frac{u_s/2-u_o}{U_C}\right)-1 \tag{24a}$$

$$N_L = \text{ceiling}\left(\frac{u_s/2+u_o}{U_C}\right), \quad \text{or ceiling}\left(\frac{u_s/2+u_o}{U_C}\right)-1 \tag{24b}$$

Therefore, there are four combinations of possible values of N_U and N_L, as listed in Table 1.

Voltage between point A and point B will be investigated next, since this is the maximum possible voltage that will be withstood by the transformer (i.e. when S_a of the upper half-bridge and S_b of the lower half-bridge are both turned on). First of all, it is easy to realise that the worst case scenario (i.e. U_{AB} being the highest) happens when both SMs connected by the auxiliary circuit are inserted (as shown in Fig. 4*a*), while the best case scenario happens when these two SMs are bypassed (as shown in Fig. 4*b*). On the other hand, U_{AB} always gets higher when there are fewer inserted SMs among the $N-1$ SMs that are not connected by the auxiliary circuit.

With the above two observations, it becomes clear that the highest U_{AB} happens when the case of Fig. 4*a* is coincident with combination 2 in Table 1. The expression of U_{AB} in this situation is

$$\begin{aligned} U_{AB} &= u_s - \left\{\left[\text{ceiling}\left(\frac{u_s/2-u_o}{U_C}\right)-1-1\right]\right. \\ &\quad \left.-\left[\text{ceiling}\left(\frac{u_s/2+u_o}{U_C}\right)-1-1\right]\right\}U_C \\ &= u_s - \left[\text{ceiling}\left(\frac{u_s/2-u_o}{U_C}\right)+\text{ceiling}\left(\frac{u_s/2+u_o}{U_C}\right)\right]+4U_C \end{aligned} \tag{25}$$

Since the first two terms on the right side of (25) always amount to a negative value, we have

$$U_{AB} < 4U_C \tag{26}$$

This effectively demonstrates that the voltage between the two windings of the transformer will always be $<4U_C$.

It should be noted that u_U, $u_L > 0$ has been assumed for the above discussion. For other cases, the same results as (26) can also be derived.

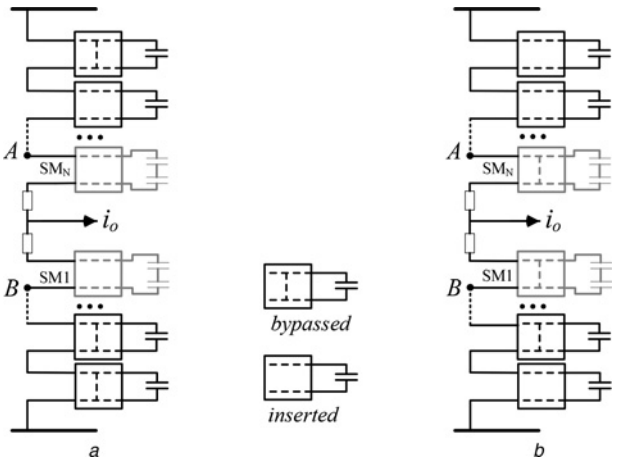

Fig. 4 *Scenarios for U_{AB}*
a Worst case
b Best case

4 Overall control system of the MMC

Shown in Fig. 5 is the overall control system of the MMC, which is used during the simulations and experiments, and which reveals mainly the outer control that deals with the control of input current, output voltage, and total leg capacitor voltage of the MMC. The inner control discussed in the previous section is also denoted in Fig. 5 to highlight its place in the overall control system.

Seen from the grid side, the MMC is like a traditional PWM rectifier. Therefore, a dual-loop (capacitor voltage outer loop and grid current inner loop) control structure commonly used with PWM rectifiers is employed here. The goal of the dual-loop control structure is to maintain U_C^{Σ} at its reference level while keeping unity power factor at the grid side. If necessary, a similar dual-loop control structure can also be used for the output side (i.e. the 'inverter' part) of the MMC. For simplicity, open-loop control is adopted for the output voltage.

Since reference $U_C^{\Sigma *}$ is a constant, a proportional–integral (PI) controller is used in the voltage outer loop. The transfer function of the PI controller is

$$G_{\text{PI}} = k_{up} + \frac{k_{ui}}{s} \tag{27}$$

where k_{up} and k_{ui} are the proportional and integral gains of the PI controller, respectively. To make the total capacitor voltage U_C^{Σ} less susceptible to sudden changes of load current I_o, feed-forward component I_{ff} is added to the outer loop

$$I_{\text{ff}} = \frac{U_o^* I_o \cos(\beta)}{U_S} \tag{28}$$

where β is power factor angle of the load.

The current inner loop forces the input current to follow its reference i_s^*. Since the latter is a sinusoid in steady state, a quasi-proportional-resonant (PR) controller [25] is employed, the

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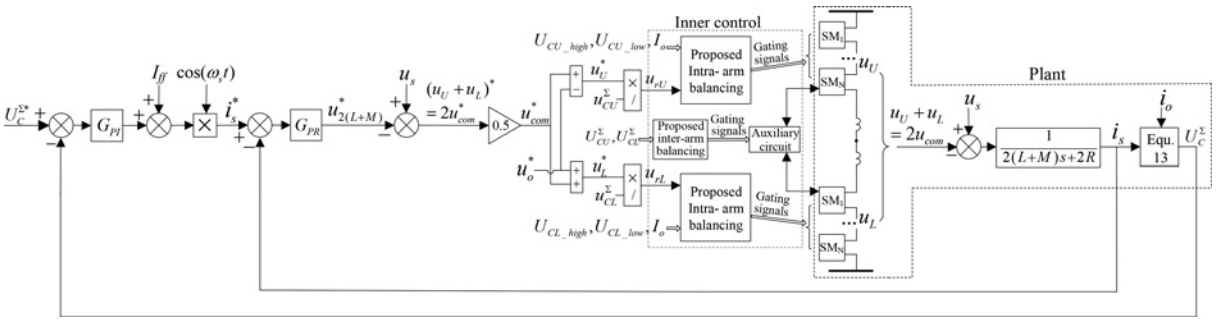

Fig. 5 *Overall control block diagram of the MMC system*

Table 2 Key parameters for simulation

Items	Symbols	Values
grid voltage (rms)	U_s	25 kV
grid frequency	f_s	50 Hz
rated power	P	2 MW
output voltage	U_o	13 kV
output frequency	f_o	1 kHz
SM capacitance	C	2000 μF[a]
rated capacitor voltage	U_C	7000 V
number of SMs per arm	N	4
self-inductance of arm inductor	L	7.3 mH
mutual inductance of arm inductor	M	6.8 mH
load resistance	R_{load}	85 Ω
carrier frequency	f_c	2 kHz

[a]Two 4000 μF ones in series for the two SMs connected by the auxiliary DC–DC converter

transfer function of which is

$$G_{PR} = k_{ip} + \frac{2k_{ir}\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{29}$$

where ω_o is the resonant frequency (equal to the grid frequency in this case). ω_c is called cutoff frequency [26], which enlarges the passband of the controller so as to make the system more robust against frequency mismatch in practical applications. The output of the current controller, $u^*_{2(L+M)}$, is the intended voltage drop across inductor $2(L+M)$ shown in Fig. 2*b*. With feed-forwarded grid voltage u_s, the reference voltage $2u^*_{com}$ of the equivalent rectifier, or intended sum of upper- and lower-arm voltages, is obtained.

Fig. 5 also depicts the process in which modulating signals u_{rU} and u_{rL} are derived from $2u^*_{com}$. The modulating signals then go

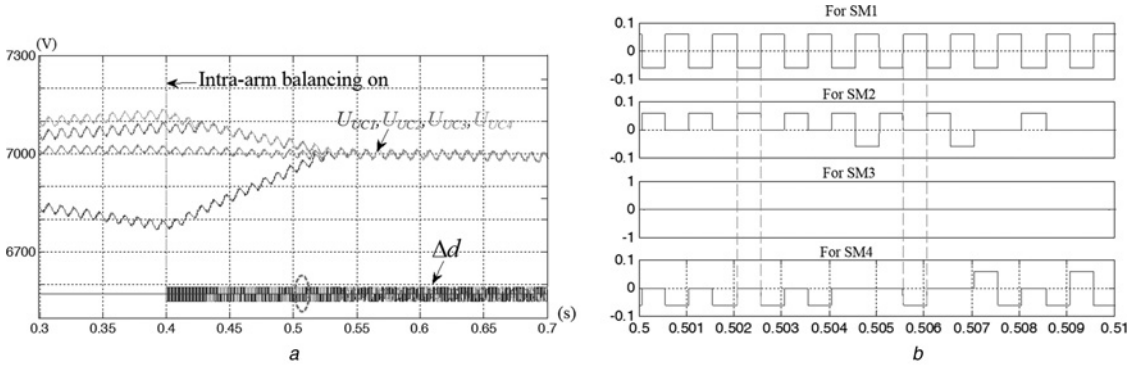

Fig. 6 *Simulation results of the proposed intra-arm voltage-balancing method*

a Upper-arm SM capacitor voltages and compensating component in the modulating signal without/with proposed intra-arm balancing method
b Enlarged view of circled area in Fig. 6*a*

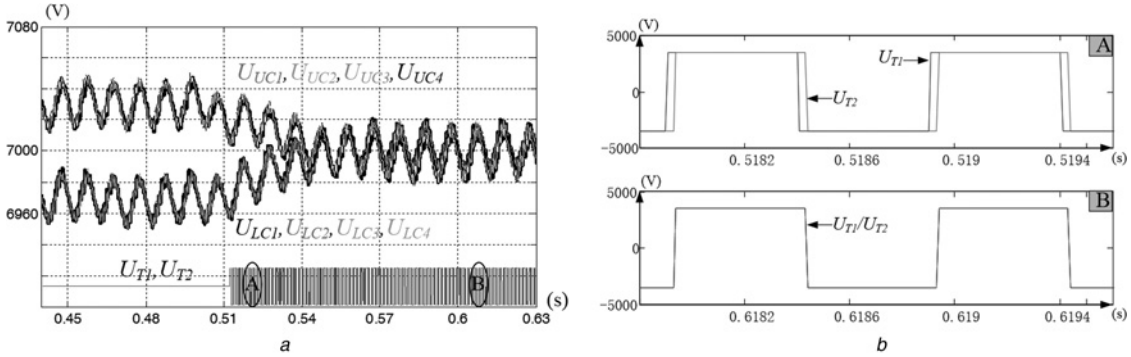

Fig. 7 *Performance of the proposed inter-arm balancing method*

a SM capacitors voltages of both arms and voltages across the windings of auxiliary transformer without/with proposed inter-arm balancing methods
b Enlarged views of the circled areas in Fig. 7*a*

Table 3 Circuit parameters for experiment

Items	Symbols	Values
grid voltage (rms)	U_S	150 V
grid frequency	f_S	50 Hz
rated power	P	300 W
output voltage	U_o	100 V
output frequency	f_o	1 kHz
SM capacitance	C	500 μF[a]
rated capacitor voltage	U_C	100 V
number of SMs per arm	N	2
self-inductance of arm inductor	L	1.2 mH
mutual inductance of arm inductor	M	1.0 mH
load resistor	R_{load}	20 Ω
carrier frequency	f_c	4 kHz

[a]Two1000 μF ones in series for the two SMs connected by the auxiliary DC–DC converter

through the proposed intra-arm voltage-balancing control to generate the gating signals for the SMs. In the meantime, inter-arm voltage balancing is carried out with proper control of the bidirectional DC–DC converter.

5 Simulation and experimental results

5.1 Simulation results

To verify the proposed mathematical model, the voltage-balancing methods, and the overall control system, a Matlab/Simulink model is built, with key parameters listed in Table 2. The 7000 V SM capacitor voltage is chosen to reduce the number of SMs, so as to reduce the complexity of the simulation model. In practice this voltage should be much lower to facilitate the use of commercially viable power devices.

Fig. 6*a* shows the simulation results of the proposed intra-arm voltage-balancing method. Initially, there are significant differences among the four SM capacitor voltages of the upper arm. After the intra-arm voltage-balancing control is activated at 0.4 s, these voltages converge to the set value of 7000 V quickly and smoothly. The modification components for the modulation signals of the four SMs are also presented, with the enlarged view of the circled area shown in Fig. 6*b*. As can be seen from Fig. 6*b*, there are only two non-zero compensations at any time, which are complementary to each other. This avoids influence on the arm voltages.

Fig. 7*a* demonstrates the performance of the proposed inter-arm balancing method. It can be seen that after the balancing control is activated at 0.5 s, the initial differences between the SM capacitor voltages of the upper and lower arms ($U_{UC1} \sim U_{UC4}$, $U_{LC1} \sim U_{LC4}$) quickly converge to a negligible level. It is also important to note that during this transient process, there are no noticeable differences between the capacitor voltages of the two SMs that are connected by the auxiliary DC–DC converter (U_{UC4} and U_{LC1}) and those of the other SMs, which is due to a successful coordination between the inter-arm balancing control and the intra-arm balancing control, as described in Section 3. Fig. 7*a* also shows the voltages across the primary and secondary windings of the transformer (U_{T1}, U_{T2}) in the auxiliary DC–DC converter, with the enlarged views of the circled areas separated shown in Fig. 7*b*.

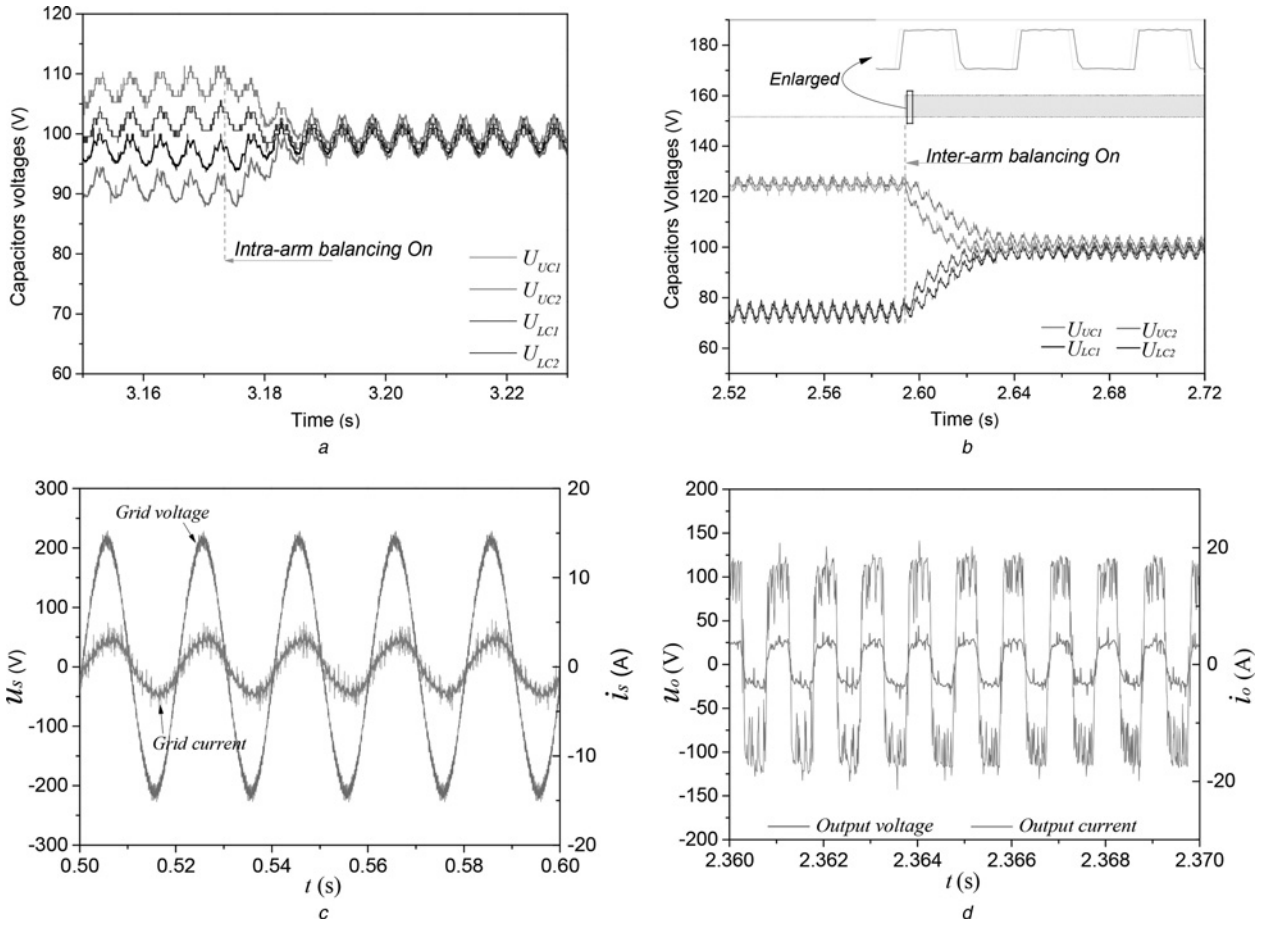

Fig. 8 *Experimental waveforms with proposed intra- and inter-arm voltage-balancing methods*

a SM capacitor voltages in one leg without and with the proposed intra-arm balancing method (experimental result)
b SM capacitor voltages in one leg, and the gating signals for upper IGBTs (*Sa*1,*Sa*2) of two half-bridge modules of auxiliary circuit without and with the proposed inter-arm balancing method
c Input voltage and current
d Output voltage and current

5.2 Experimental results

A test set-up of the single-phase AC–AC MMC is built, with the key parameters listed in Table 3. The medium-frequency transformer and the AC–DC–AC railway drive that follow the MMC in Fig. 1*a* are replaced with a resistive load in the experiments. The control hardware employs digital signal processors (DSPs) and field-programmable gate arrays (FPGAs), with most of the control calculation implemented in the DSPs and generation of PWM signals implemented in the FPGAs.

Fig. 8*a* shows the experimental waveforms of intra-arm voltage balancing for the upper and lower arms.

Fig. 8*b* shows the experimental waveforms of inter-arm voltage balancing, including the driving signals for the upper insulated-gate bipolar transistor (IGBTs) (*Sa*1, *Sa*2) of the two half-bridges of the auxiliary DC–DC converter.

Shown in Fig. 8*c* and *d* are the input voltage/current and output voltage/current. The input current is controlled according to unity power factor. The output voltage is control as a 1 kHz square wave. There is noticeable switching ripple in the output voltage since it is directly feeding the resistive load without any filtering.

6 Conclusion

Intra-arm and inter-arm balancing methods are proposed for a single-phase AC–AC MMC for railway drive applications. The proposed intra-arm balancing method is based on CPSPWM, which combines the advantages of both CPSPWM- and PDPWM-based methods. The proposed inter-arm balancing method is based on an auxiliary circuit, which decouples balancing control with arm voltages, therefore does not affect the input/output power quality. With the two balancing strategies working together to guarantee an even distribution of SM capacitor voltages, a simplified mathematical model is also established for the single-phase AC–AC MMC, which reveals the power transfer relationship more clearly and serves as a basis for selecting proper strategies for outer-layer control system of the MMC. Simulation and experimental results verify the effectiveness of mathematical model and voltage-balancing method.

7 Acknowledgments

This work was supported by the National Natural Science Foundation of China (Project No. 51477063) and the Power Electronics Science and Education Development Program of Delta Environmental & Educational Foundation (Project No. DREG2014013).

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